ABSTRACT:

A data processing device has load and store instructions which address memory with the content of a data pointer register. In a normal mode, the same data pointer register is used for all load and store instructions. In this mode the processor is compatible with a older processor design. In a special mode, at least two different registers are used alternately to address memory when memory access instructions are executed. A control register controls whether or not the different registers are updated as part of the memory access instructions. Preferably, the control register provides for more than one different kind of update of the different registers, such as post addressing increment, post addressing decrement etc.

Fig. 1